New Linearization Method for the Modulated Signals with High Peak-to-average Ratio: Peak-to-Average Ratio Reduction and Expansion

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Abstract— **A new linearization method for the high power amplifier modulated by a high peak-to-average ratio signal is proposed. The amplifier consists of a high power amplifier with a predistorter, a peak power limiter, and cancellation loops similar to the feedforward amplifier. The linearization performance is enhanced by reducing the peak input power to the amplifier using a rate limiter and the distortion from the limited signal is restored at the cancellation sub-path. Simulation and experimental results for the amplifier module with WCDMA signal show a significant improvement of ACLR.**

I. Introduction

Modern communication systems employ spectrum efficient modulation techniques, such as CDMA, WCDMA, OFDM, etc. The modulated signals have complicated signal statistics and high peak-to-average ratios [1]-[4]. The signal statistics inherently affect the nonlinear behavior of high power amplifiers, and circuit configurations for linearization of the power amplifiers should be adopted to the signal statistics including peak-to-average ratio(crest factor). Therefore, to achieve the required performance efficiently, appropriate linearization strategies for each modulation scheme should be applied. Generally, feedforward and various kinds of predistortion circuits have been most widely used to linearize high-power amplifiers . The expected performances and limitations of these techniques are well-documented in the previous research works [4]-[9]. A proper choice or combination of the technologies with some modifications are required to achieve various specifications of the amplifiers for linearity, efficiency, cost, and size, etc.

The feedforward is still considered to be the best performing linearization technique. However, it has many drawbacks, such as complexity, production-ability, efficiency, size, and so on, which result in cost problems. For 3rd generation wireless systems, the linearity specifications, especially adjacent channel leakage ratio(ACLR) and out-of-band spectrum emission(abbreviated as SE in this paper), become tighter than those of the 1st or 2nd generation systems. Therefore, a linearization technique which is simpler and more productionable than feedforward but provides a better performance than predistortion, is highly desired.

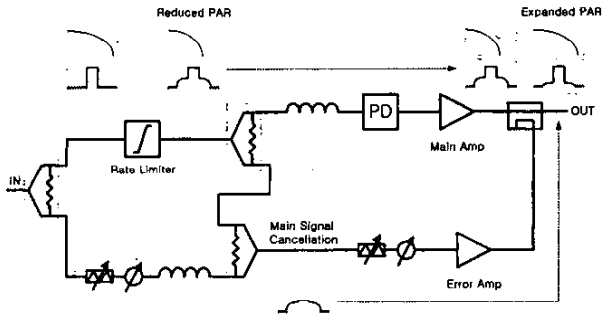

Fig. 1. Operational diagram of PRE(Peak-to-average ratio Reduction and Expansion) amplifier module

In this paper, a new linearization scheme is proposed for this purpose and demonstrated. In this scheme, the peak-to-average ratio of the input signal to the amplifier is reduced by using a rate limiter. After amplification, two cancellation loops restore the modulated signals with a high peak-to-average ratio. The power amplifier operates more linearly at the reduced power level and linearity is further improved through the restoration process. This technique has been verified using base-band system simulation and demonstrated experimentally with a downlink WCDMA signal having 8.6dB peak-to-average ratio at 0.1% CCDF(Complementary Cumulative probability Density Function) at 2.14GHz band.

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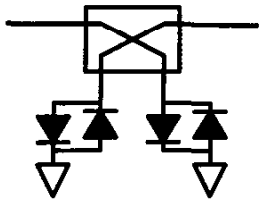


Fig. 2. The circuit diagram of the rate limiter used in this experiment

II. Operation Principle of PRE

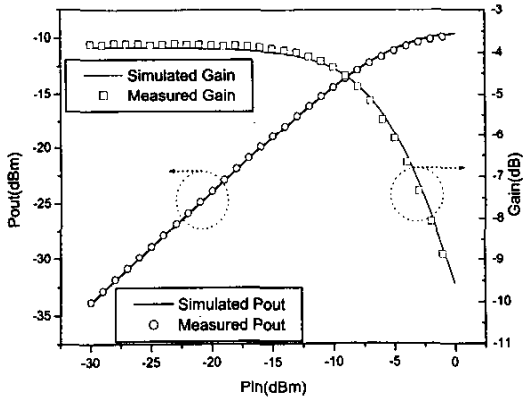
Operational diagram of the proposed PRE(Peak-to-average ratio Reduction and Expansion) amplifier is shown in Fig. 1. The circuit configuration is very similar to the feedforward amplifier with two cancellation loops. However, the locations of the main amplifier and the delay line of the PRE amplifier are different from those of the feedforward amplifier and its operation principle is quite different. The main power amplifier module consists of a predistorter and high-power amplifier. The peak power of the input signal to the amplifier module is reduced by the rate limiter. The predistorter delivers a better linearization as the PAR(Peak-to-Average Ratio) of the signal decreases. The power amplifier also generates less spectral regrowth as the PAR decreases at the same average output power. Therefore, the linearity of the amplifier module will be enhanced.

The power clipping process generates a high spectral regrowth, i.e. out-of-band spectrum emission, and this distorted signal is amplified by the module. This distortion component is eliminated by the two cancellation loops. The cancellation process is identical to the feedforward amplifier. The distortion component due to the limiting is extracted at the signal cancellation loop. Next, it is compensated at the error cancelling loop, restoring the distortion of the output signal of the amplifier module. We have successfully demonstrated the superior performance of the PRE amplifier using the class AB operated silicon LDMOSFET amplifier.

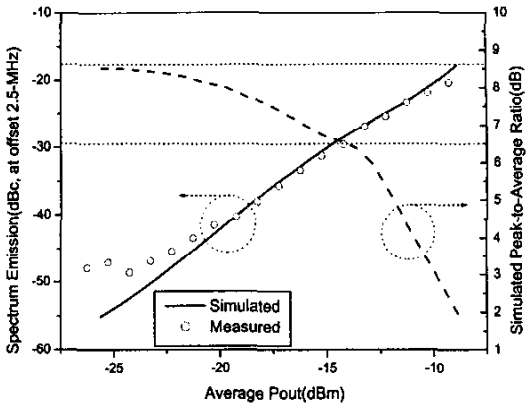
III. Implementation of PRE Amplifier Circuit

To validate this linearization scheme, the PRE amplifier shown in Fig. 1 was built using 30W-PEP class AB silicon LDMOSFET as a main amplifier(using Motorola's MRF21030 LDMOSFET) and 10W-PEP class AB silicon LDMOSFET as an error amplifier module.

In this experiment, a compact predistorter is used for linearization of the power amplifier. The circuit diagram of the rate limiter used in this experiment is given in Fig. 2. The circuits are configured using 90^o hybrid and Schottky diodes, and is a reflection type. The simulated and measured performances of the rate limiter are presented in Fig. 3. Fig. 3(a) shows the simulated and measured gain and power responses of the rate limiter. The simulation is performed using a harmonic balance method in ADS. The measured and simulated gain responses show very good limiting characteristics. Fig. 3(b) shows the simulated and measured spectrum emission at 2.5MHz offset using a WCDMA signal for a broad output power level. It also shows the simulated PARs versus the output power levels. As the output power level increases, the spectrum emission increases and PAR decreases. The cancellation



(a)



(b)

Fig. 3. The simulated and measured performances of the rate limiter: (a) the simulated and measured gain and power responses and (b) the simulated and measured spectrum emission at 2.5MHz offset and the simulated PARs through an average output power level of WCDMA signal

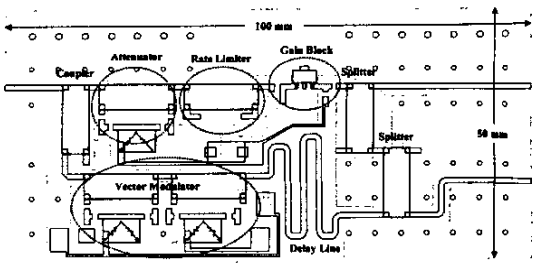


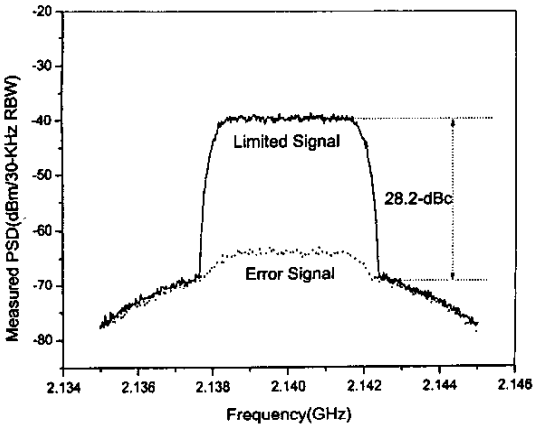
Fig. 4. Layout of the cancellation block including the rate limiter

loop to extract the error signal generated by the PAR reduction process was designed and implemented in a single block. The layout of the cancellation block which includes the rate limiter is shown in Fig. 4. The size of the cancellation block is 100mmX50mm, which is very compact in comparison to that of the feedforward. The delay line is easily implemented using a micro-strip on the circuit board due to a small delay difference between the two paths and the low power level.

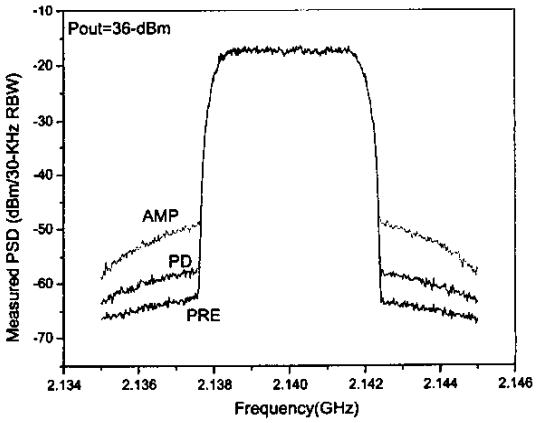
IV. Experimental Results and Discussions

The experiments were conducted to demonstrate the linearity improvement of the PRE amplifier module using 30W-PEP LDMOSFET. For ease of comparison using explicit measurement data, the following evaluations were sequentially performed. First, the amplifier characteristics using WCDMA signal was measured. Second, the characteristics of the power amplifier module with the predistorter by applying WCDMA signal were optimized by adjustment of the amplitude and phase of the IM terms of the predistorter and the performances are measured. Finally, the linearization characteristics of the PRE module for the amplifier module with the predistorter were evaluated.

The results of the above three measurements are presented in Fig. 5 and 6. Fig. 5(a) provides the measured power spectral densities for the output signal of the rate limiter, i.e. after PAR reduction. Fig. 5(b) shows the measured power spectral densities for the output signal of the amplifier alone, the amplifier with the predistorter, and the PRE module at 36dBm of the output power level, As shown, ACLR is clearly improved with PRE operation. Fig. 6 summarizes the measured results for the power-level-dependent ACLR improvements. The spectrum emissions at 2.5MHz offset for the amplifier, amplifier with predistorter, and PRE module are plotted through a broad power level. At the optimized power level of 36dBm, the overall improvement for linearity is 14.47dB, about 9.18dB by the predistorter and an additional improvement of 5.29dB from



(a)



(b)

Fig. 5. (a) the measured PSDs of the output signals from the rate limiter and from the cancellation block and (b) the measured PSDs of the output signals from the amplifier, amplifier with predistorter, and PRE module at the 36dBm of output power level

the PRE operation. The linearization mechanism of the PRE is independent from the predistorter. Therefore, the linearization performance is improved by the PRE technique and is further enhanced by a predistortion method. This technique is fully applicable to the multi-carrier amplifiers, as well as the single-carrier amplifiers, due to its capability to handle a broad bandwidth.

In view of the circuit complexity, the limiting block and error amplifier are added to the conventional amplifier module with a predistorter. This becomes more complex than predistortion method, but is much simpler than

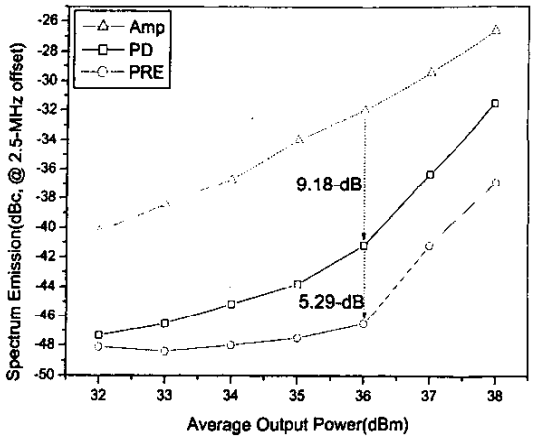


Fig. 6. The measured spectrum emissions at 2.5MHz offset from the amplifier and the PD amplifier module with the source signal input, and from the PRE amplifier module

the feedforward amplifier. It has no delay line or delay filter at the high-power output path, which can cause a fatal output power loss and size or complexity problems. It has only very simple signal cancellation circuits because the circuits linearize the very small size and low power limiter, which has been demonstrated in our experiments. Additionally, the main amplifier is automatically protected from the input over-drive by the rate limiter, which is an another subsidiary merit of the PRE amplifier. However, the employed error amplifier can be a burden for cost and efficiency. Overall, the PRE technique is an improved version of a predistortion amplifier for high PAR signals using a simpler ciruit configuration than the feedforward amplifier.

V. Conclusions

A new linearization method for the modulated signal with a high peak-to-average ratio has been proposed and demonstrated. It is based on the reduced peak power level for amplifier input and the signal is restored by the cancellation loops after amplification. The PAR reduction using a rate limiter causes a considerable amount of spectral regrowth, but the main amplifier module with the predistorter operates more linearly at the reduced peak power level. The spectral regrowth generated by the PAR reduction process is suppressed using the cancellation loops similar to the feedforward circuits. The difference is that it linearizes the limiter nonlinearity.

The PRE amplifier module has many advantages compared to the conventional predistortion and feedforward amplifiers. These have been addressed in section II and IV. The PRE method of linearization could be an intermediate technique between the predistortion and feedforward from the viewpoints of linearization performance and complexity. Linearity improvement can be better than the conventional predistorter because two layers of linearization techniques are employed, i.e., predistortion and error cancellation. However, the circuit configuration is much simpler than that of feedforward amplifier because it linearizes the small power limiter. This technique can be implemented to any type of predistorter, including the baseband correction method because the linearization mechanism is independent from predistortion linearization.

Experiments have been carried out using a high power class AB amplifier at a 2.14GHz band. The experimental results proves the feasibility of the PRE amplifier. Therefore, this technique will be a viable approach for linear amplifier design with an enhanced performance over the predistortion amplifier but with a relatively simple circuit configuration.

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